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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,900	02/26/2002	Vipul Anil Desai	CR00249M	2757

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EXAMINER	
STEELMAN, MARY J	
ART UNIT	**PAPER NUMBER**
2191	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,900	DESAI ET AL.	
	Examiner	Art Unit	
	Mary J. Steelman	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Remarks and Amendments received 12 April 2005. Per Applicant's request, claims 13 and 16 have been amended. Claim 15 has been canceled. Claims 1-14 and 16 are pending.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: The oath references "Title 37, Code of Federal Regulations, Section 1.56(a)", should be --...1.56...--. Remove the '(a)' See MPEP Chapter 2000 - Duty of Disclosure, 37 CFR 1.56.

Regarding the submission of an amended declaration in the Remarks, only the signature pages were submitted / and or scanned into the PTO files.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 6,061,521 to Thayer et al..

Per claim 1:

A method of forming a compound Single Instruction/Multiple Data instruction, said method comprising:

(Thayer: Single Instruction/Multiple Data instructions are vector instructions (col. 7, lines 1-4) where "an operation can be performed on each operand concurrent with operations on other operands." Thayer disclosed the combination of two operations, thus a compound single instruction, multiple data instruction. Thayer disclosed 'compound Single Instruction/Multiple Data instructions (SIMD): (col. 8, lines 65-67), "The present invention further contemplates an MEU (multimedia extension unit-functions as a DSP) capable of executing two distinct sets of operations within a single instruction cycle." Additionally, col. 11, lines 62-65, col. 12, lines 15-16, col. 17, lines 5-15, and col. 20, lines 34-35, disclose more examples of combining two dissimilar types of operations to process during one cycle (forming a compound SIMD).)

-selecting at least two Single Instruction/Multiple Data operations of a reduced instruction set computing type;

(Thayer: Col. 11, lines 62-65, col. 12, lines 15-16, col. 17, lines 5-15, and col. 20, lines 34-35, disclose more examples of combining two dissimilar types of operations to process during one cycle (forming a compound SIMD). Col. 11, line 67-col. 12, line 2, "Thus, if IDCT (inverse discrete consign transform) requires more than one operation type be performed during each instruction cycle, two operation types are available to enhance IDCT throughput." If the

processing algorithm requires multiple operations, two operations may be selected and combined in one instruction cycle. Thayer suggested using a 'reduced instruction set computing type' at col. 12, lines 15-16.)

-combining said at least two Single Instruction/Multiple Data operations to execute in a single instruction cycle to thereby yield the compound Single Instruction/Multiple Data instruction. (Thayer: See FIG. 4, the columns under #78, #84, and #86 where addition and subtraction operations are combined in an instruction cycle.)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,061,521 to Thayer et al., in view of US Patent 6,513,146 B1 to Yonezawa et al.

Per claim 2:

-evaluating a processing throughput of the compound Single Instruction/Multiple Data instruction;

(Thayer: Single Instruction/Multiple Data instructions are vector instructions (col. 7, lines 1-4) where "an operation can be performed on each operand concurrent with operations on other operands." Thayer disclosed the combination of two operations, thus a compound single instruction, multiple data instruction. Thayer disclosed 'compound Single Instruction/Multiple Data instructions (SIMD): (col. 8, lines 65-67), "The present invention further contemplates an MEU (multimedia extension unit-functions as a DSP) capable of executing two distinct sets of operations within a single instruction cycle." Additionally, col. 11, lines 62-65, col. 12, lines 15-16, col. 17, lines 5-15, and col. 20, lines 34-35, disclose more examples of combining two dissimilar types of operations to process during one cycle (forming a compound SIMD). Thayer gave consideration to efficient throughput (col. 1, line 15) and disclosed the desire to perform operations in parallel, using minimal instruction cycles (col. 6, lines 28-33).)

Thayer failed to disclose the relationship of efficient throughput to power consumption. However, Yonezawa disclosed:

-determining a power consumption of the...instruction;

(Yonezawa: Abstract, lines 3-8, "...power consumption of each function is estimated through an operation description analysis of functions...so as to determine S/W and H/W implementation. Col. 3, lines 60-61, "...analyzing power consumption...", col. 4, line 5, "...estimating power consumption..." when determining the design of an integrated circuit and partitions software and hardware (col. 16, lines 16-24).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the

invention to modify Thayer's invention that combines operations in a vector (SIMD) instruction to increase efficiency, by modifying features as disclosed by Yonezawa to determine the power consumption, because both inventions give consideration to throughput (Thayer, col. 1, line 15 and Yonezawa, col. 1, lines 19-20) which directly affects power consumption in the design of efficient integrated circuits.

Per claim 3:

Regarding the limitations:

-associating an energy consumption value with at least one micro-operation of the compound Single Instruction/Multiple Data instruction;

Thayer disclosed 'compound Single Instruction/ Multiple data instruction. See rejection of claim 2 above. Thayer failed to disclose 'associating an energy consumption value with at least one micro-operation.'

However, Yonezawa disclosed the relationship of energy consumption with at least one micro-operation: Col. 2, lines 45-50, "...obtaining power consumption of each function by analyzing functions included in a system operation description language describing operation (micro-operations)...")

Thayer failed to disclose:

-minimizing the sum of the energy consumption value.

However, Yonezawa disclosed: Col. 2, lines 50-54, "...partitioning the function into a H/W implemented function when the power consumption of the function exceeds a threshold value

and into a S/W implemented function when the power consumption is smaller than the threshold value...")

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Thayer's invention that uses compound SIMD instructions while giving consideration to throughput (col. 1, line 15) by combining features as disclosed by Yonezawa to determine the power consumption, because both inventions give consideration to throughput (Yonezawa, col. 1, lines 19-20). Efficient throughput directly is related to power consumption, and a worthy consideration in the design of a circuit device (Yonezawa, col. 1, line 11-14).

7. Claims 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,061,521 to Thayer, in view of "SPONSOR'S FEATURE – DSP PROCESSORS Power and efficiency Architectures for this Century's applications", by Richard Oed and Marcus Gossler (Summer 2001 / Texas Instruments).

Per claims 4-12:

-the compound Single Instruction/Multiple Data instruction includes a vector add-subtract operation / a vector minimum-difference operation / a vector compare-maximum operation / a vector absolute difference and add operation / a vector average operation / a vector scale operation / a vector conditional negate and add operation / a vector select and viterbi shift left operation.

Thayer disclosed a 'vector add-subtract operation' as a type of compound Single Instruction/Multiple Data instruction. See FIG. 4, columns under #78, #84, and #86. Thayer disclosed various operations useful in multimedia processing (col. 6, lines 55-56col. 7, lines 18-32, col. 8, lines 29-30, col. 10, lines 23-25. Thayer failed to disclose other specific operations of the system.

However, Oed and Gossler disclosed (page 1, paragraph 4) "Two new dsp architectures...satisfy the demand for calculation power...and power efficiency..."
Page 1, paragraph 9, "The improvement in code efficiency is based on the fact that the new processor generation does not used fixed length instructions...they can now use words...New instructions have been added to allow more operations in parallel, ..These parallel instructions are supported by functional units like a second multiply accumulate unit and a second arithmetic logic unit..." Page 2, paragraph 2, "his improvement has been achieved by extending the cpu core – allowing better parallelism – and by adding special image processing instructions...a risc architecture...Algorithms like vector product, Reed-Solomon decoding or motion estimation can be speeded by a factor of seven." Page 2, paragraph 4, "Additionally, the chip has a Viterbi coprocessor..."

Thus, Oed and Gossler disclosed instructions combined into words, newly added instructions, a RISC architecture, and the Viterbi operation. Instructions are added to allow more operations in parallel. Page 1, paragraph 2, "...support has been added to dsps for such features as circular addressing – needed by digital filters – and hardware for loop constructs. This led to several dsp

families each specializing in a certain area."

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Thayer by giving consideration to Oed and Gossler who disclosed specialized operation instructions to satisfy the need for calculation power and power efficiency (page 1, paragraph 4), as Thayer disclosed consideration to efficient throughput (col. 1, line 15) as desirable to process multimedia type algorithms (col. 4, lines 2-5).

8. Claims 13, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,513,146 B1 to Yonezawa et al., in view of US Patent 6,061,521 to Thayer et al.

Per claim 13:

A method of estimating a relative power consumption of a software algorithm ...

(Yonezawa: Col. 1, line 52-53, "...method of designing a semiconductor integrated circuit...", col. 1, lines 47-48, "...by using a processing quantity and power consumption as parameters (estimating relative power consumption)..."

-establishing a relative energy database listing a plurality of micro-operations, each micro-operation having an associated relative energy value;

(Yonezawa: Col. 25, lines 65-67, "FIGs. 27(a) through 27(c) are tables (relative energy database) for respectively showing a power analysis result, the power information an a power

analysis result obtained after changing the program..." Micro operations such as set, add, mul, mov, ret, as shown in the drawings, are related to power consumption.)

-determining the relative power consumption...incorporating one or more or the micro-operations based on the relative energy values of the incorporated micro-operations. (Yonezawa: See Fig. 27(a) shows the power consumption before optimizing. Fig. 27(c) shows the power consumption of the software algorithm after a shift operation has replaced a mul operation.)

Yonezawa failed to address specifically a "plurality of compound Single Instruction/Multiple Data instructions of a reduced instruction set computing type (RISC)..." However, Thayer disclosed 'compound Single Instruction/Multiple Data instructions (SIMD): (col. 8, lines 65-67), "The present invention further contemplates an MEU (multimedia extension unit-functions as a DSP) capable of executing two distinct sets of operations within a single instruction cycle." As an example, Thayer suggests the x86 CPU (col. 7, line 65, a reduced instruction set computing type / RISC). Additionally, col. 11, lines 62-65, col. 12, lines 15-16, col. 17, lines 5-15, and col. 20, lines 34-35, disclose more examples of combining two dissimilar types of operations to process during one cycle (compound SIMD). Single Instruction/Multiple Data instructions are vector instructions (col. 7, lines 1-4) where "an operation can be performed on each operand concurrent with operations on other operands." Thayer disclosed the combination of two operations, thus a compound single instruction, multiple data instruction.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Yonezawa's invention related to consideration of power consumption when designing a circuit, by including compound SIMD instructions on a RISC computing type because Thayer recognized the need to enhance the throughput (col. 1, line 15). Col. 6, lines 30-34, "It would be desirable to perform as many operation-intensive computations as possible in parallel, and within as few instruction cycles as possible." Col. 10, lines 22-24, "Vector instructions...enhance DSP throughput...while avoiding unnecessary operations." Enhanced throughput contributes to reduced power consumption, a design consideration (col. 20, line 21) in the Yonezawa reference. While Yonezawa was suggestive of any type of circuit device (col. 1, line 13), Thayer disclosed a more specific RISC type.

Per claim 14:

-executing the software algorithm on a simulator;

(Yonezawa: Col. 23, lines 9-15, "...instruction set simulator (ISS) is a simulator for conducting simulation in accordance with instructions of a program...the instruction set simulator is aggregate of software having functions to conduct the same operations as the microcomputer", col. 24, lines 48-49, "The power analysis system of this example functions as an instruction set simulator.")

-computing a sum of the relative energy values of the micro-operations contained in the executed software algorithm.

(Yonezawa: Col. 2, lines 54-57, "...calculating a sum of the power consumption of all of the

functions as total power consumption by estimating the power consumption of each function..." See FIGs. 27(a)-27(c). Analysis / sum of relative energy values of the micro-operations.)

Per claim 16:

A method for estimating the absolute power consumption of a software algorithm, comprising:

-determining a plurality of relative power estimates of instructions of a microprocessor;

(Yonezawa: Col. 2, lines 47-50, "...obtaining power consumption of each function by analyzing functions included in a system operation...". Col. 2, lines 56-57, "...estimating the power consumption of each function...")

-simulating a software algorithm...;

(Yonezawa: Col. 4, lines 36-37, "...power analyzing means for conducting simulation (simulating)...in accordance with the source program (software algorithm)...")

-determining an absolute power estimate of a software algorithm to be executed by the microprocessor based on the relative power estimates.

(See rejection of limitations as addressed in claims 13 and 14 above.)

Yonezawa failed to explicitly disclose "absolute power consumption." Yonezawa did disclose (col. 4, lines 34-40) "power information storing means for storing power information...and power analyzing means for conducting simulation...and analyzing power consumed in executing

the source program...", which broadly may infer "estimating the absolute power consumption". Yonezawa failed "one or more compound Single Instruction/Multiple Data instructions of a reduced instruction set computing type". However, Thayer disclosed (col. 11, lines 62-65, col. 12, lines 15-16, col. 17, lines 5-15, and col. 20, lines 34-35) examples of combining two dissimilar types of operations to process during one cycle (forming a compound SIMD). Col. 11, line 67-col. 12, line 2, "Thus, if IDCT (inverse discrete consign transform) requires more than one operation type be performed during each instruction cycle, two operation types are available to enhance IDCT throughput." If the processing algorithm requires multiple operations, two operations may be selected and combined in one instruction cycle. Thayer suggested using a 'reduced instruction set computing type' at col. 12, lines 15-16.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Yonezawa's invention to include "absolute power consumption."

Response to Arguments

9. Applicant has argued, in substance, the following:

(A) As Applicant has noted on page 5, 4th paragraph of Remarks, received 12 April 2005, in reference to claim 13, Yonezawa fails to teach "determining the relative power consumption of the plurality of compound Single Instruction/Multiple Data instructions incorporating one or more of the micro-operations based on the relative energy values of the incorporated micro-operations."

Examiner's Response: These are newly added limitations. See rejection of claim 13 above. Thayer disclosed compound Single Instruction/Multiple data instructions.

(B) As Applicant has noted on page 6, 3rd paragraph of Remarks, regarding claim 1, the reference teaches away from "combining said at least two Single Instruction/Multiple Data operations to execute in a single instruction cycle to thereby yield the compound Single Instruction/Multiple Data instruction."

Examiner's Response: See rejection of claim 1 above. Thayer disclosed combining two operations in a vector instruction (compound Single Instruction/Multiple Data instruction).

(C) As Applicant has noted on page 9, 1st paragraph of Remarks, regarding claims 4-12, the cited art fails to teach "a specific compound SIMD instruction."

Examiner's Response: Thayer disclosed compound SIMD instructions.

(D) As Applicant has noted on page 10, 1st paragraph of Remarks, regarding claim 16, Yonezawa fails to teach "simulating a software algorithm including one or more compound Single Instruction/Multiple Data instructions of a reduced instruction set computing type."

Examiner's Response: These are newly added limitations. Thayer disclosed compound SIMD instructions of a reduced instruction set computing type. See rejection of claim 16 above.

Conclusion

10. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Also note:

US Patent 5,649,179 to Steenstra et al.

Steenstra disclosed a method for programming and controlling SIMD processors by dynamically allocating instructions. "The first step...it to parse...instruction targeted for the SIMD processor into components that effect the operation of a given processing element...In step 2, the

components are assembled into a control specification for the processing element decoder (col. 2, lines 24-28)". Col. 1, lines 19-22, "The disadvantage of wide instruction words...increases power consumption..." Col. 5, lines 41-51, "The dynamic allocation of instructions to processing elements in a SIMD processor is advantageous...the SIMD processor instruction word length can be minimized..."

US Patent 5,818,788 to Kimura et al.

Kimura disclosed, using a SIMD architecture, "the order of issued addresses can change, be shifted, in order to minimize the number of word addresses changed, and the order can be restored to the original sequence after a memory access...(col. 6, lines 5-9)." "With the above mentioned arrangement, a high-speed, low-power and highly-stable logic integrated...SIMD architecture can be realized (col. 6, lines 9-11)." Kimura alters accesses to registers or memory blocks using the clock with a timing skew to reduce the peak current flow (col. 6, lines 50-65).

US Patent 6,151,568 to Allen et al.

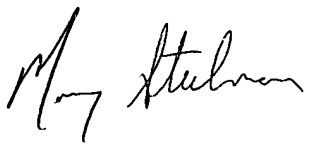
Allen disclosed an invention that analyzes and calculates power consumed (col. 2, lines 28-29), generates power consumption estimation (col. 2, line 53), using a simulator (col. 2, line 56), and writes to a scenario database (col. 5, line 50).

US Patent 6,513,145 to Venkitakrishnan.

Venkitakrishnan disclosed a method for estimating the maximum power consumed, estimating power consumption by modeling a benchmark, summarizing the results (Abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman 

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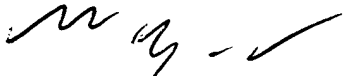

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